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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,162	02/29/2000	Koji Hirayama	572.38256X00	1546

20457 7590 02/18/2004

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EXAMINER	
PHAN, TRI H	
ART UNIT	**PAPER NUMBER**
2661	9

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/516,162	HIRAYAMA ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6 and 8* is/are pending in the application.

4a) Of the above claim(s) *2,7 and 9-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Arguments

1. This Office Action is in response to the Response/Amendment filed on December 01st, 2003. Claims 2, 7 and 9-17 are now canceled. Claims 1, 3-6 and 8 are now pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In regard to claim 3, the recitation "*said control processor*" in line 2 is vague and indefinite. There are insufficient antecedent basis for this limitation in the claims 1 and 3.

Also in claim 3, the recitation "*said processor*" in line 6 is vague and indefinite because it is unclear whether the limitation refers to the processor in the "*plural kinds of signal processors*" (claim 1, line 15) or the "*control processor*" (claim 3, line 2) or the "*plural kinds of processors*" (claim 3, lines 2-3) or the "*other processor*" (claim 3, line 5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ueda et al.** (U.S.5,359,600) in view of **Kato** (U.S.6,529,523).

- In regard to claim 1, **Ueda** discloses in Figs. 1-4 and in the respective portions of the specification about the ATM self-routing switch ("*communication apparatus for transferring information*") in the ATM switching system ("*ATM network*") includes a plurality of incoming trunk circuits with STM-ATM receive interface units ("*plural kinds of interfaces*") which convert the STM-N and ATM incoming signals ("*communication signals*") into ATM cells ("*ATM cells*") inputted at the inlets ("*input ports*") and outputted at the outlets ("*output ports*") of the ATM self-routing switch ("*ATM switch*") to the one of the outgoing trunk circuits (For example see Col. 2, Lines 11-61) specified by the VPI ("*based on the header information of the ATM cell*") as disclosed in Col. 3, Lines 33-36. **Ueda** does discloses about the STM-ATM incoming trunk circuits which convert the STM-N and ATM incoming signals ("*communication signals*") into ATM cells as a common "*signal format or protocol*" and about the maintenance and management system ("*control part*") provided to determine and control the routing plan of the traffic in the system (For example see Col. 2, Lines 50-61), but fails to specifically disclose

about the "*second interface*" for receiving ATM cells and "*plural kinds of signal processors*" for converting the incoming signals. However, such implementation is known in the art.

For example, **Kato** discloses in Figs. 1-8, 13 and in the respective portions of the specification about the converting circuits and bandwidth management apparatus in the mixing STM and ATM networks with a plurality of STM and ATM line interfaces ("*first and second interfaces*"; For example see Fig. 13), wherein the processor CPU at each line interfaces ("*plural kind of signal processors*") controls the process at each unit such as the converting circuit and timing circuit for the STM signals based on the information of the header (For example see Col. 5, Lines 17-51; Col. 6, Lines 48-57; Col. 8, Lines 19-52; Col. 9, Line 15 through Col. 10, Line 16).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Kato** by implementing the different line interfaces for STM-N and ATM incoming signals and each processor for each switch unit into the incoming trunks of the **Ueda**'s system, with the motivation being to improve the ability to convert and manage the bandwidth and timing for each unit in the mixing network, e.g. STM and ATM networks, for the purpose of providing reliability and reducing the cost and processing time at the ATM switch.

- Regarding claim 5, the combination of the **Ueda** and **Kato**'s system does disclose about the mixing networks, e.g. STM and ATM networks, but fails to specifically disclose about the IP network. However, ATM switch is a well known packet-like switching, which can be used in associated with different network protocols and Internet Protocol is well known in the art for

transporting the IP packets; therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use an IP interface with converting the IP packets into ATM cells in the incoming trunk circuits of the **Ueda** and **Kato**'s system, with the motivation being to provide the ATM switch with different protocols in the mixing network disclosed in the combination of the **Ueda** and **Kato**'s system.

- In regard to claims 6 and 8, the combination of the **Ueda** and **Kato**'s system does disclose about the converting circuit for converting TDM frames of the STM network to cells, passing through the ATM switch, and converting circuit for converting cells of the ATM network to TDM frames of the STM network, where the cells/frames are sent to prescribed terminal (For example see **Kato**: details in Figs. 8-9; Abstract). **Ueda** fails to specifically disclose about the "*second interface*" for receiving ATM cells, converting the control signals and outputting to the ATM switch. **Kato** discloses about the converting circuits and bandwidth management apparatus in the mixing STM and ATM networks with a plurality of STM and ATM line interfaces ("*first and second interfaces*"), wherein the processor CPU at each line interfaces controls the process at each unit such as the converting circuit and timing circuit for the STM signals ("*control signal*") based on the information of the header with reading and writing of address data to and from the control memory at period of the time slots, converts into ATM cells and pass to the ATM switch (For example see Figs. 8-9 and 12-13; Col. 5, Lines 17-51; Col. 6, Lines 48-57; Col. 8, Lines 19-52; Col. 9, Line 15 through Col. 10, Line 16).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Kato** by implementing the

different line interfaces for STM-N and ATM incoming signals and each processor for each switch unit into the incoming trunks of the **Ueda**'s system, with the motivation being to improve the ability to convert and manage the bandwidth and timing for each unit in the mixing network, e.g. STM and ATM networks, for the purpose of providing reliability and reducing the cost and processing time at the ATM switch.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ueda et al.** (U.S.5,359,600) in view of **Kato** (U.S.6,529,523), and further in view of **Mano** (U.S.6,012,151).

- Claim 3 is rejected under 35 U.S.C. 112, second paragraph, set forth in this Office action, as in Part 3 above, but in the interest of expediting the examination process, the examiner will interpret the recitation "*said control processor*" of the claimed invention as 'said control part' as predefined in claim 1.

- In regard to claims 3 and 4, the combination of **Ueda** and **Kato**'s system discloses all the subject matter of the claimed invention as discussed in part 5 of this Office action above, about the ATM self-routing switch in the ATM switching system includes a plurality of incoming trunk circuits with STM-ATM receive interface units, which convert the STM-N and ATM incoming signals into ATM cells as a common format or protocol, inputted at the inlets and outputted at the outlets of the ATM self-routing switch to the one of the outgoing trunk circuits specified by the VPI and about the maintenance and management system provided to

determine and control the routing plan of the traffic in the system as **Ueda** discloses; about the converting circuits and bandwidth management apparatus in the mixing STM and ATM networks with a plurality of STM and ATM line interfaces, wherein the processor CPU at each line interfaces controls the process at each unit such as the converting circuit and timing circuit for the STM signals based on the information of the header. The combination of **Ueda** and **Kato**'s system discloses about the write/read controller 40 and read/write controller; each provides different control for reading and writing of address data to and from the control memory at period of the time slots and where the routing unit 56 ("*second ATM switch*") adds the destination information into the header for performing switching cells to destination (For example see **Kato**: Fig. 8, Col. 9, Line 15 through Col. 10, Line 16), but fails to specifically disclose about the "*plural kinds of processors*" at the maintenance and management system. However, such implementation is known in the art.

For example, **Mato** discloses in Figs. 1-2, 14, and 39-40 and in the respective portions of the specification about the information processing apparatus and distributed processing control method, in which a plurality of processors are used for improving the redundancy, reliability and efficiency in performing the distributed load processing (For example see Col. 1, Lines 8-23); wherein the plurality of call processors 51-1 to 51-n ("*plural kinds of processors*") associated with the operation and maintenance processor ("*control part*") in the ATM switch for process requests of the input and output ports in the distributed manner (For example see Figs. 14 and 40; Col. 15, Lines 7-17; Col. 27, Lines 26-67) and a plurality of signal processors 71-1 to 71-n ("*plural kinds of signal processors*") for transferring the control of data transferred and accommodating input/output signals, e.g. "*ATM cells*", between the input and output ports, e.g.

"*first and second interfaces*", (For example see Figs. 39-40; Col. 26, Line 66 through Col. 27, Line 25; Col. 27, Lines 26-67).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Mato,** which implements a plurality of signal processors and call processors at the input ports and at the maintenance and management system in **Ueda** and **Kato**'s system, with the motivation being to improve the redundancy, reliability and efficiency in performing the distributed load processing in distributed manner of the ATM switch.

Response to Arguments

7. Applicant's arguments filed on December 01st, 2003 have been fully considered but they are not persuasive.

In regard to claim 1, Applicant argues that the combination of **Ueda** and **Kato**'s system fails to disclose the communication apparatus including plural kinds of first interfaces for converting plural kinds of control signals or communication signals from plural kinds of communication networks, except the ATM network, to ATM cells, a second interface for receiving an ATM cell to which a control signal or a communication signal is inserted from the ATM network, plural kinds of signal processors, connected to the ATM switch, for converting a signal output from the first and second interfaces to a signal format or protocol used by each of the plural kinds of communication networks and a control part for receiving the ATM cell, which

is output from one of the plural kinds of signal processors and to which a control signal is inserted through the ATM switch, and performing a necessary processing among plural kinds of processing. Examiner respectfully disagrees. **Ueda** discloses about the ATM self-routing switch ("*communication apparatus for transferring information*") in the ATM switching system ("*ATM network*") includes a plurality of incoming trunk circuits with STM-ATM receive interface units ("*plural kinds of interfaces*") which convert the STM-N and ATM incoming signals ("*communication signals*") into ATM cells ("*ATM cells*") inputted at the inlets ("*input ports*") and outputted at the outlets ("*output ports*") of the ATM self-routing switch ("*ATM switch*") to the one of the outgoing trunk circuits specified by the VPI ("*based on the header information of the ATM cell*") and about the STM-ATM incoming trunk circuits which convert the STM-N and ATM incoming signals ("*communication signals*") into ATM cells as a common "*signal format or protocol*" and about the maintenance and management system ("*control part*") provided to determine and control the routing plan of the traffic in the system. **Kato** discloses about the converting circuits and bandwidth management apparatus in the mixing STM and ATM networks with a plurality of STM and ATM line interfaces ("*first and second interfaces*"), wherein the processor CPU at each line interfaces ("*plural kind of signal processors*") controls the process at each unit such as the converting circuit and timing circuit for the STM signals based on the information of the header. Therefore, Examiner concludes that the combination of **Ueda** and **Kato**'s system teaches the arguable features.

Claims 3-6 and 8 are rejected as in Part 5 and 6 above of this Office action and by virtue of their dependence from claim 1.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kunimoto et al. (U.S.5,303,236), **Uchida et al.** (U.S.5,239,593), **Tanabe et al.** (U.S.6,314,096), **Juntumaa et al.** (U.S.6,430,189), **Hayashi** (U.S.6,091,736), **Takatori et al.** (U.S.5,577,037) and **Nam et al.** (U.S.6,081,535) are all cited to show devices and methods for improving switching architectures with the ATM communication network, which are considered pertinent to the claimed invention.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.

Tri H. Phan
February 12, 2004